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Yet another problem associated with the prior embodiments is that each of the graphics devices has to calculate the shape of each and every object on the frame. Each device must calculate each object's shape in order to determine whether or not the object, or a portion of the object, must be further processed by the graphics engine associated with the graphics device. An associated problem is that when an object straddles the demarcation line between an area that the first graphics device is to process and an area that the second graphics device is to process, it is necessary for both devices to process the object. For example, when a portion of an object is in the top half of the screen, and a portion on the bottom half of the screen, calculations associated with the object are calculated by both graphic devices.

Please replace the paragraph beginning at Page 3, line 19, with the following rewritten paragraph:

a3
Yet another problem with the known implementations of multiple graphic devices is the need to carefully match the digital-to-analog converters (DACs) associated with each VGA. The DACs of each VGA provide a plurality of voltages, one for each video component, such as the red/green/blue components. If the DACs are not carefully matched, it is possible for colors viewed on a display device to have slightly different shades of color because of the lack of calibration between the devices' DACs.

Please replace the paragraph beginning at Page 8, line 8, with the following rewritten paragraph:

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The Comparator 220 provides an output signal labeled COMPARE SIGNAL. The COMPARE SIGNAL will indicate when a match occurs between the voltage of the color component signal G and the VREF signal. In general, the COMPARE SIGNAL will toggle from an inactive state indicating the signals do not match to an active state indicating that the signals have matched. It will be understood by one of ordinary skill in the art that if the Comparator 220 were to comprise a simple differential amplifier, the COMPARE SIGNAL would maintain the active state indicating a match, even when the green signal attains a voltage level significantly higher than the VREF signal. In other words, in the embodiment illustrated, the toggling of the signal COMPARE SIGNAL from one state to another indicates a match has occurred. The signal labeled ADJUST CONTROL is received by the Adjust Signal Generator 230. The Adjust

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Signal Generator 230, in response to a signal from Control 130 received as part of the ADJUST SIGNAL CONTROL, provides a signal labeled ADJUST SIGNAL. In a specific embodiment, the ADJUST SIGNAL GENERATOR 230 is a variable reference source. The ADJUST SIGNAL provides a value for calibrating the DAC values of at least one of the VGAs.

Please replace the paragraph beginning at page 9, line 4, with the following rewritten paragraph:

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In operation, at least a portion of the VGA1 CONTROL signal is received by the first video controller 310. As illustrated, the VGA1 CONTROL signal comprises N signals that are received by the first video-out controller. In addition, the VGA1 Control signals are received by the Synchronize Device 350. It should be noted that M and N may be the same value. Likewise, the signal VGA2 CONTROL is received by the second video-out controller labeled VIDEO OUT2 CONTROL 320, and the Synchronize Device 350. Information transmitted over the LOCAL BUS is also received by the video-out controllers 310 and 320. It should be noted that information over the Local Bus will generally be received by the controller 130 at a single port, whereby the data can be provided to one or both of the two video-out controllers as appropriate.

Please replace the paragraph beginning at page 10, line 21, with the following rewritten paragraph:

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At step 420, the first signal is provided to a first node. With reference to Figure 1, the node is one of the plurality of nodes carrying the RGB1 signal. It should be noted that in the embodiment illustrated, that the RGB1 signal is provided to a bus comprising three nodes, one for each color component. Likewise, the RGB2 signal is provided to a bus comprising a node for each color component.

Please replace the paragraph beginning at page 10, line 26, with the following rewritten paragraph:

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Next, at step 430, a value associated with the first signal and the first output node is determined. With reference to Figures 1 and 2, the signal RGB OUT1 is provided to the Multiplexor 210 of Figure 2. One of the RGB signals is chosen at the analog Multiplexor 210 of Figure 2, and provided to the Comparator 220. In the specific implementation illustrated, the

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values of the color components associated with the RGB OUT1 signal are voltage values. In other implementations, values other than voltages, i.e. current values, can be provided to Video-Out Adjust 160 of Figure 1. A specific implementation for determining the value during step 430 is to have the first VGA 110 change the value of the monitored color component (green in this example) until the value received at Comparator 220 matches VREF. This is accomplished by having the Controller 130 indicate to the VGA 110 to change the digital value of the DAC. By changing the digital DAC value the value received at the Comparator 220 of Figure 2 will also change. By monitoring the compare signal associated with the Comparator 220, the digital DAC value at which the first signal in step 420 matches VREF can be determined.

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Please replace the paragraph beginning at page 11, line 12, with the following rewritten paragraph:

At step 440, a second signal is generated at a second graphics device. With reference to Figure 1, the signal being generated would be the RGB2 signals by VGA 120. When the RGB1 signal and the RGB2 signals are to provide alternating frames of video to Video Port1, it is necessary to compensate the values of the two VGAs 110 and 120 so that their RGB output values are approximately the same for given digital DAC value. If the output voltages of RGB1 and RGB2 are not the same for a given DAC value, variations in color will be detectable when switching occurs between VGAs 110 and 120. Therefore, at step 440, the color component signal that is to be calibrated to the first signal will be generated using the value determined in step 430.

Please replace the paragraph beginning at page 14, line 3, with the following rewritten paragraph:

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Figure 5 illustrates another method in accordance with the present invention. At step 510, a first signal is generated representing a first color component of a first frame, and a second signal is generated representative of the first color component for a third frame of video. The first and second signals are both generated on a first VGA. With reference to Figure 1, the first and second video signals can be generated by the first VGA 110.

Please replace the paragraph beginning at page 14, line 20, with the following rewritten paragraph:

a-10 In accordance with the present invention, the steps 510 through 550 are advantageous in that the workload distribution is approximately even because each VGA processes an entire frame of video, each frame of data is sent only one time to one VGA, each shape of a frame is calculated only once by one VGA, and there is no straddle data to burden down both processors. In addition, the voltage equalization as described within the method of Figure 2 also provides the advantage of allowing for even color reproduction regardless of the VGA driving an output port.

Please replace the paragraph beginning at page 14, line 27, with the following rewritten paragraph:

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a-11 It should be further understood that the specific steps of Figures 4 and 5 can actually be implemented in hardware and/or in software. For example, the various steps of generating signals can be performed by a hardware engine of the graphics controllers 110 and 120, or the steps can be performed in firmware, such as in microcode, executed on the processing engine associated with the controllers 110 and 120, or it may even be performed fully in software on a central processing unit. In general, a system for rendering video may include a processing module and memory. The processing module may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcontroller, digital signal processor, microcomputer, portion of the central processing unit, state machine, logic circuitry, and/or any device that manipulates signals (e.g., analog or digital) based on operational instructions. The memory may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, floppy disk memory, magnetic tape memory, erasable memory, portion of system memory, and/or any device that stores operational instructions in a digital format. Note that when the processing module implements one or more of its functions via a state machine or logic circuitry, the memory storing the corresponding operational instructions is embedded within the circuitry comprising the state machine and/or logic circuitry.
